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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,783	WANG ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Extension of Time as received on 8/15/2006.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner suggests incorporating the idea of register renaming and the insertion of a select instruction into the title. MPEP 606.01 states "This may result in slightly longer titles, but the loss in brevity of title will be more than offset by the gain in its informative value in indexing, classifying, searching, etc. If a satisfactory title is not supplied by the applicant, the examiner may, at the time of allowance, change the title by examiner's amendment."

4. The disclosure is objected to because of the following informalities: On page 9, line 23, replace "propogates" with --propagates--.

Appropriate correction is required.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: On page 9, lines 1

and 3, applicant refers to stage 210, which is not found in the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to because Fig.7A, step 756, refers to a "uOF". Does applicant instead mean --uOP-- as shown in step 760? Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not

accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-8 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, regarding claims 1 and 14:

a) applicant is claiming that register renaming is deferred for a plurality of registers defined by predicated instructions upon which a common/dependent instruction depends until at least one register corresponding to the predicated instructions is renamed. It is not clear from the claim, which registers applicant is talking about. Looking at Fig.6, the inserted select instruction appears to only defer renaming for the mov instruction. And, the mov instruction includes only a single register (not a plurality of registers) that is defined by predicated instructions (the source, which in this example, is renamed to rD). If applicant is referring to other registers, then it should be made clear.

b) applicant claims that renaming is deferred by the inserted micro-operation until at least one register corresponding to the predicated instructions is renamed. The select operation does not appear to include any registers corresponding to predicated instructions that are renamed. Instead, it appears as if predicated instructions have registers which are renamed and then those registers are used as sources in the inserted instruction. Consequently, the only register

corresponding to the predicated instruction that is renamed is the registers in the predicated instruction. Looking at Fig.6, however, the inserted select operation does not defer renaming until these registers are renamed as this renaming happens before the select operation is inserted.

In general, the examiner feels that claims 1 and 14 are not clear and should be reworded to accurately claim applicant's invention.

9. Claim 2 recites the limitation "the pipeline instruction" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

10. Claims 3-8 and 15-16 are also rejected under 35 U.S.C 112, 2nd paragraph for being indefinite because they are dependent on claims that are indefinite.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-6 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dabbagh et al., U.S. Patent No. 6,701,425 (herein referred to as Dabbagh).

13. Referring to claim 1, Dabbagh has taught a microprocessor comprising:

a) a unit to insert a first micro-operation into an instruction stream. See column 6, line 42, to column 7, line 8. Note that a send guard instruction is inserted into the stream to transfer the predicate/guard value to the unit that needs to analyze the predicate. In an alternate

interpretation, any other instruction inserted between a producer and consumer will qualify as the first micro-operation.

b) while injecting the first micro-operation does inherently defer processing of subsequent instructions, Dabbagh has not taught deferring renaming of a plurality of registers defined by predicate instruction upon which a common instruction depends until at least one register corresponding to the predicated instructions is renamed. However, Official Notice is taken that register renaming is a well-known concept which allows for a reduction in hazards, and consequently, processor stalling. Clearly, if an extra instruction is injected into the stream, then the processing is stalled at least one clock cycle for all subsequent instructions. And, since renaming, which is known to occur before dispatching, is part of the processing pipeline, the renaming would be deferred at least a cycle as well. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a register renamer for renaming registers accessed by instructions. In addition, as disclosed by Dabbagh, a sendguard operation is inserted when an instruction requiring the reading of a predicate is encountered, where the instruction is stalled (until the guard/predicate is received) in A_IDQ 41 or in ARLQ 111 or in store address queue 71, which are all subsequent to the dispatch stage 99 (see Fig.1 of Dabbagh and column 6, lines 42-47). Consequently, the stalled instruction is renamed prior to dispatching and then stalled while waiting for the sendguard. Any dependent instruction after the sendguard, which defers all processing and renaming of instructions after it by at least one cycle, will have its renaming deferred until at least one register corresponding to the predicated instructions is renamed (i.e., at time X when the at least one register is renamed or after), which is the case because the register in the predicated instruction is already renamed.

Furthermore, it should be realized that any subsequent instruction could access registers defined by a predicated instruction. For instance, the program may have two consecutive predicated arithmetic operations, one which writes to register R1 and another which writes a result to register R2. Then a consumer instruction could follow, if the programmer so desires which reads both R1 and R2, performs an arithmetic operation on them, and then stores the result in register R3. Therefore, merely claiming an instruction sequence is not a patentable feature. An infinite number of program sequences may exist and it is known to have consumers follow producers. And, in a system with register renaming, consumers must have their registers renamed as well.

c) as discussed above Dabbagh has not taught a plurality of register renaming units (or an augmented register alias table) to rename at least one register corresponding to the predicated instructions wherein the common instruction is to use data from a plurality of destination registers corresponding to the first micro-operation. However, for the reasons discussed above, this is also an obvious modification to Dabbagh. It would be obvious to have register renaming units (and augmented alias table) to track and rename registers corresponding to predicated instructions. A consumer will also be using data from a destination register that is associated with the predicate that is transferred by the first micro-operation (in the case of a send guard instruction) or may be a consumer of the first micro-operation (reads the producer's destination).

14. Referring to claim 2, Dabbagh has taught a microprocessor as described in claim 1. Furthermore, if Dabbagh includes register renaming as set forth above, then Dabbagh also has taught that a register renaming unit renames each one of a plurality of source registers of the pipeline instruction and renames a destination register to a new physical register. This is another concept that occurs with register renaming. Each original destination is renamed to a new

destination, and subsequent instructions that access the original destination as a source, must have that source renamed to the new destination as well.

15. Referring to claim 3, Dabbagh has taught a microprocessor as described in claim 2. Furthermore, if Dabbagh includes register renaming as set forth above, then Dabbagh also has taught that the augmented register alias table includes a plurality of lines and wherein each one of the plurality of lines includes a plurality of renamed destination registers. Again, if a renaming system is employed, then there must be a table which tracks and maps the registers.

16. Referring to claim 4, Dabbagh has taught a microprocessor as described in claim 3. Dabbagh has further taught that each one of a plurality of select-uops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier. Clearly, Dabbagh executes arithmetic-type operations such as Adds and Subs (Fig.1). These operations are known to access multiple source registers.

17. Referring to claim 5, Dabbagh has taught a microprocessor as described in claim 4. Dabbagh has further taught that the plurality of source operands comprises a first source operand and a plurality of secondary source operands. Again, it is known that when an ADD instruction is executed, two operands may be two register operands (add two numbers to get a result).

18. Referring to claim 6, Dabbagh has taught a microprocessor as described in claim 5. Dabbagh has further taught that the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available. The ADD instruction source must be valid and available otherwise the program would execute with incorrect data (and produce incorrect results).

19. Referring to claim 14, Dabbagh has taught a computer system comprising a processor, wherein the processor includes:

a) a unit to insert a first micro-operation into an instruction stream. See column 6, line 42, to column 7, line 8. Note that a send guard instruction is inserted into the stream to transfer the predicate/guard value to the unit that needs to analyze the predicate. In an alternate interpretation, any other instruction inserted between a producer and consumer will qualify as the first micro-operation.

b) the first micro-operation to defer renaming of a plurality of registers defined by different predicated instructions, upon which a dependent instruction depends until at least one register corresponding to the predicated instruction is renamed. However, Official Notice is taken that register renaming is a well-known concept which allows for a reduction in hazards, and consequently, processor stalling. Clearly, if an extra instruction is injected into the stream, then the processing is stalled at least one clock cycle for all subsequent instructions. And, since renaming, which is known to occur before dispatching, is part of the processing pipeline, the renaming would be deferred at least a cycle as well. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a register renamer for renaming registers accessed by instructions. In addition, as disclosed by Dabbagh, a sendguard operation is inserted when an instruction requiring the reading of a predicate is encountered, where the instruction is stalled (until the guard/predicate is received) in A_IDQ 41 or in ARLQ 111 or in store address queue 71, which are all subsequent to the dispatch stage 99 (see Fig.1 of Dabbagh and column 6, lines 42-47). Consequently, the stalled instruction is renamed prior to dispatching and then stalled while waiting for the sendguard. Any dependent

instruction after the sendguard, which defers all processing and renaming of instructions after it by at least one cycle, will have its renaming deferred until at least one register corresponding to the predicated instructions is renamed (i.e., at time X when the at least one register is renamed or after), which is the case because the register in the predicated instruction is already renamed. Furthermore, it should be realized that any subsequent instruction can access registers defined by a predicated instruction. For instance, the program may have two consecutive predicated arithmetic operations, one which writes to register R1 and another which writes a result to register R2. Then a consumer instruction could follow, if the programmer so desires which reads both R1 and R2, performs an arithmetic operation on them, and then stores the result in register R3. Therefore, merely claiming an instruction sequence is not a patentable feature. An infinite number of program sequences may exist and it is known to have consumers follow producers. And, in a system with register renaming, consumers must have their registers renamed as well.

c) a plurality of execution units to execute the dependent instruction. See Fig.1.

d) While Dabbagh has not explicitly taught a reorder buffer, Official Notice is taken that reorder buffers are well known in the art. They allow for the reordering of instructions that have been executed out of order, which further allows for increased throughput. As a result, it would have been obvious to implement a reorder buffer in Dabbagh to achieve out of order execution.

e) as mentioned above, Dabbagh has not taught a plurality of register renaming units (or augmented register alias table) to rename at least one register corresponding to a predicated instruction, wherein the dependent instruction is to use data from a plurality of destination registers corresponding to the first micro-operation. However, for the reasons discussed above, this is also an obvious modification to Dabbagh. It would be obvious to have register renaming

units (and augmented alias table) to track and rename registers corresponding to predicated instructions. A consumer will also be using data from a destination register that is associated with the predicate that is transferred by the first micro-operation (in the case of a send guard instruction) or may be a consumer of the first micro-operation (reads the producer's destination).

f) Dabbagh has not taught a plurality of reservation stations, however Official Notice is taken that reservation stations are well known in the art. They provide efficient operand tracking and scheduling of instructions. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Dabbagh to include a plurality of reservation stations.

g) wherein a register renaming unit, the reorder buffer, the plurality of execution units, and the plurality of reservation stations are coupled to at least one of a plurality of dynamic pipeline stages. it is inherent that all logic in a processor is coupled to a pipeline, which is inherently made of stages.

h) a system bus. See Fig.1

i) a computer memory system. See Fig.1, Fig.3, and Fig.4.

j) an input/output device. See the register files of Fig.1. Registers receive input and supply output and are therefore I/O devices.

k) wherein the system bus is coupled to the processor, the computer memory system and the input/output device. See Fig.1.

20. Referring to claim 15, Dabbagh has taught a computer system as described in claim 14. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 3.

21. Referring to claim 16, Dabbagh has taught a computer system as described in claim 15. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 2.

22. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dabbagh, as applied above, in view of Fetterman et al., U.S. Patent No. 5,553,256 (herein referred to as Fetterman).

23. Referring to claim 7, Dabbagh has taught a microprocessor as described in claim 5. While Dabbagh has inherently taught that each operand includes a physical status identifier (the registers must be identified via address specifier), Dabbagh has not taught that each one of the plurality of second source operands includes a plurality of status bits. However, Fetterman has taught associating status bits with register operands to track their progress. See Fig.2, bits S1V and S2V, column 9, lines 40-42, and column 4, lines 52-58, and note that one bit tracks readiness and the other tracks when it's been written to (commit bit).

24. Referring to claim 8, Dabbagh in view of Fetterman has taught a microprocessor as described in claim 7. Dabbagh in view of Fetterman has further taught that the plurality of status bits has a ready bit and a committed bit. See the rejection of claim 7.

Allowable Subject Matter

25. Claims 9-13 are allowed.

Response to Arguments

26. Applicant's arguments filed on August 15, 2006, have been fully considered but they are not persuasive.

27. Applicant argues the novelty/rejection of claims 1 and 14 on pages 8-9 of the remarks, in substance that:

> "In order to fully support the rejection, the Office Action takes "Official Notice" that it would be obvious to one of ordinary skill in the art to use the "send guard" instruction of Dabbagh to defer renaming of the plurality of registers defined by predicated instructions. Yet, the Office Action provides no teaching that the send guard instruction of Dabbagh is used this way, either within Dabbagh or another reference. Instead, the Office Action merely asserts that it would be obvious to use the send guard instruction to defer the renaming of the plurality of registers as claimed in claims 1 and 14.
>
> This is classic impermissible hind-sight reconstruction of claims 1 and 14. In order to support an obviousness rejection under 35 U.S.C. 103, the Office Action must, inter alia, provide a reference teaching each element of the rejected claim and some motivation within the references to combine the references. Not only does the Office Action not provide a reference that teaches using a uop to defer renaming of a plurality of registers defined by a predicated instruction, but the Office Action provides not motivation to combine any such references."

28. These arguments are not found persuasive for the following reasons:

a) The examiner is only asserting that register renaming is well known and that it would be obvious to implement in Dabbagh. Simply by adding it, deferred renaming for anything following a sendguard instruction would result. This must happen because if you insert a sendguard instruction into the stream at time X, then the original instruction supposed to be processed at time X must now wait to be processed until time X+Y. And, the instruction that was to be originally processed at time X+Y must now wait until time X+Z, and so on, thereby creating a domino effect. Since the processing would include the renaming, the renaming is deferred for each instruction after the inserted sendguard instruction. The examiner asserts that a reference does not need to be supplied which shows a sendguard specifically used to defer register renaming. Only a reference showing that register renaming is known will be supplied. And, by having register renaming implemented in Dabbagh, a result would be deferred renaming when a sendguard is inserted. An analogy is cutting in line. If somebody cuts in line, then the people behind the cutter must wait longer for service (i.e., their service is deferred by the amount

of time required to serve the cutter). Similarly, if a sendguard instruction is inserted, then renaming is to be deferred for those instructions behind the sendguard instruction. For support that register renaming results in the reduction of hazards, which clearly leads to a reduction in stalling, see Hennessy and Patterson, "Computer Architecture - A Quantitative Approach, 2nd Edition," 1996, pp.251-252.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
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October 18, 2006

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